

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: FORMING TAPERED LOWER ELECTRODE PHASE-
CHANGE MEMORIES

INVENTOR: DANIEL XU

Express Mail No. EL911616889US

Date: OCTOBER 11, 2001

FOR "E915260"

FORMING TAPERED LOWER ELECTRODE PHASE-CHANGE MEMORIES

Background

This invention relates generally to memories that use phase-change materials.

5 Phase-change materials may exhibit at least two
different states. The states may be called the amorphous
and crystalline states. Transitions between these states
may be selectively initiated. The states may be
distinguished because the amorphous state generally
10 exhibits higher resistivity than the crystalline state.
The amorphous state involves a more disordered atomic
structure and the crystalline state involves a more ordered
atomic structure. Generally, any phase-change material may
be utilized; however, in some embodiments, thin-film
15 chalcogenide alloy materials may be particularly suitable.

 The phase-change may be induced reversibly.
Therefore, the memory may change from the amorphous to the
crystalline state and may revert back to the amorphous
state thereafter or vice versa. In effect, each memory
20 cell may be thought of as a programmable resistor, which
reversibly changes between higher and lower resistance
states in response to temperature changes. The temperature
changes may be induced by resistive heating.

09975163.101101

09975163 .101101

In some situations, the cell may have a large number of states. That is, because each state may be distinguished by its resistance, a number of resistance-determined states may be possible, allowing the storage of multiple bits of data in a single cell.

A variety of phase-change alloys are known. Generally, chalcogenide alloys contain one or more elements from column VI of the periodic table. One particularly suitable group of alloys are GeSbTe alloys.

10 In any memory, it is desirable to pack the individual memory cells as closely as possible. With conventional phase-change memory materials, there is no real way to self-align the trenches that separate adjacent rows of memory cells from one another. Therefore, critical

15 alignment processing may be necessary to accurately space one wordline from the next. Moreover, extra real estate may be needed between adjacent wordlines to make up for any misalignment between the trenches and the adjacent memory cells.

20 Thus, there is a need for better ways to form trenches for phase-change memories.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view in accordance with one embodiment of the present invention;

25 Figure 2 is an enlarged cross-sectional view of the structure described in Figure 1 at an early stage

fabrication, in accordance with one embodiment of the present invention;

Figure 3 is a cross-sectional view of the embodiment depicted in Figure 2 after subsequent processing;

5 Figure 4 is a cross-sectional view of the embodiment depicted in Figure 3 after further processing;

Figure 5 shows subsequent processing on the structure shown in Figure 4 in accordance with one embodiment of the present invention;

10 Figure 6 shows subsequent processing on the structure shown in Figure 5, in accordance with one embodiment of the present invention;

Figure 7 shows subsequent processing on the structure shown in Figure 6 in accordance with one embodiment of the present invention;

15 Figure 8 is an enlarged, cross-sectional view of the structure shown in Figure 7 after additional processing in accordance with one embodiment of the present invention; and

20 Figure 9 is a schematic depiction of a processor-based system in accordance with one embodiment of the present invention.

Detailed Description

25 Referring to Figure 1, in one embodiment of the invention, a memory cell 10 may include a suitable phase

change material 32 disposed between a tapered lower
electrode 22 and an upper electrode 31. One suitable type
of phase change material may be an alloy that includes at
least one chalcogen element, and a transition element among
5 others. Examples of such alloys are alloys of Germanium,
Antimony and Tellurium.

09975463.101101
The lower electrode 22 may be formed over a substrate
12. The substrate 12 may include a lower substrate portion
12a of a first conductivity type that, in one embodiment of
10 the present invention, may be a P- material. A conical
substrate portion 12b may extend upwardly from the lower
portion 12a to the lower electrode 22. The conical
substrate portion 12b may include a plurality of layers 14-
20.

15 In one embodiment, the layers 14, 16, and 18 may be of
a second conductivity type opposite to the first
conductivity type. For example, the layer 14 may be an N-
layer, the layer 16 may be an N+ layer, and the layer 18
may be an N- layer, in accordance with one embodiment of
20 the present invention. Together the layers 14, 16, and 18
may form a buried wordline, in one embodiment of the
present invention.

Over the layers 14, 16, and 18, may be a layer 20 of
the first conductivity type, which, in one embodiment of
25 the present invention, may be a P+ layer. The
juxtaposition of the layers 14, 16, and 18 of a second

conductivity type below the layer 20 of a first conductivity type may form a diode.

5 The tapered shape of the lower electrode 22 reduces the contact area between the electrode 22 and the phase-change material 32. This increases the resistance at the point of contact, increasing the ability of the electrode 22 to heat the layer 32. In some embodiments, the lower electrode 22 may be made of cobalt silicide and may be covered by interfacial layers.

10 The conical substrate portion 12b may be covered with a suitable dielectric 30 such as silicon dioxide. Further, each wordline may be electrically isolated from two adjacent wordlines by trenches 33 that may be filled with insulator 34 such as silicon dioxide.

15 The sidewalls of the conical substrate portion 12b may be covered with dielectric layers 26 and 28. In some embodiments the layer 26 may be silicon dioxide and the layer 28 may be silicon nitride. The layers 26 and 28 may aid in the formation of the trenches 33.

20 The upper electrode 31 may be made of any suitable electrical conductor. In some embodiments the electrode 31 may be covered by barrier or adhesion layers.

Turning next to Figure 2, the formation of the memory cell 10 may begin with the formation of the layers 14-20.

25 The substrate 12 may be subjected to a sequence of ion implantation steps. The energy, dose, and angle of ion

beams of a series of implants may be selected to achieve the doping profile of the layers 14, 16, 18 and 20 shown in Figure 2.

While the exact nature of the ion implantation steps
5 may be subject to considerable variation, an initial implantation may be utilized to form a P-type well. This may be followed by P type and N type implants to form the layers 14-20. These implants in turn may be followed by one or more additional implants, in some embodiments, to
10 create the profiles indicated in Figure 2. In some embodiments, P type regions may be formed by a boron implant and N type regions may be formed by a phosphorus implant.

The same implantation process may simultaneously be
15 used to define structures in a large number of surrounding memory cells (not shown) also formed in the substrate 10. This implantation process may be done in a blanket fashion without masking between cells, in some embodiments.

The lower electrode 22 may be deposited over the
20 region 20 as depicted in Figure 3. A mask 24, which may be made of photoresist, may be patterned over each electrode 22 on the substrate 12 to form circular patches, in some embodiments. The structure, shown in Figure 3, may be isotropically etched. Mask and etch parameters are
25 selected so that the vertical and lateral etch rates are sufficient to cut through layers 16, 18 and 20 and achieve

a taper on the electrode 22. The deposition of the lower electrode 22 may also simultaneously form the lower electrodes 22 of a number of surrounding memory cells (not shown) without the need to mask off the electrodes 22 for
5 each cell.

The substrate portion 12b is conically shaped as a result of the etching as shown in Figure 4. The etched dimension of the lower electrode 22 may be smaller than that of the mask 24 due to undercutting. The isotropic
10 etching also separates the electrodes 22 of each memory cell 10 from the electrodes 22 of surrounding cells. The mask 24 may be subsequently removed, for example by ashing, to expose the lower electrode 22.

In some embodiments, the size of the closed region of
15 mask 24 may be the minimum feature size attainable. Other methods to reduce the area of the upper surface of the lower electrode 22 may include reactive means such as oxidation.

The conical substrate portion 12b may be covered with
20 dielectric layers 26 and 28 as shown in Figure 5. A process such as low-pressure chemical vapor deposition (LPCVD) may be used to deposit each material. Again, the portions 12b of a large number of surrounding memory cells (not shown) may be covered in the same blanket deposition
25 without masking between the cells.

Subsequently the dielectric layer 28 may be etched selectively with respect to the dielectric layer 26 by any anisotropic means such as reactive ion etching. The residual dielectric region 28 over the conical substrate portion 12b is removed from horizontal surfaces as a result of anisotropic etching as shown in Figure 6.

Further, the conical substrate portion 12b may be covered with an insulator 30, as shown in Figure 7. This insulator 30 is chemically distinct from dielectric layer 28 and, in some embodiments, may be high-density plasma (HDP) oxide. Planarization of the insulator 30, for example, by chemical mechanical planarization (CMP) may expose (and perhaps flatten) the tip 27 of the lower electrode 22.

A pair of spaced trenches 33, electrically isolating a wordline of cells 10 from adjacent wordlines, may be etched through the insulator 30 on either side of the memory cell 10 using suitable patterning and etching methods. In particular, the etch parameters are selected to etch the insulator 30 selectively with respect to the dielectric region 28.

In regions of slight mask misalignment, the dielectric layer 28 reduces the etching of the conical substrate portion 12b confining the etch to the region between adjacent wordlines. Thus, the dielectric layers 26 and 28 enable the etching of the trenches 33 in close proximity to

the conical substrate portion 12b of surrounding memory cells 10 without the need for a critical mask alignment.

The etched trenches 33 extend into the lower substrate portion 12a to electrically isolate the wordline of cells 10. The cells in each wordline may be simultaneously severed from adjacent wordlines by severing the connection that remains via the layer 14. Thus, a plurality of wordlines may be electrically isolated by the same self-aligned trench isolation step.

Referring to Figure 8, the phase-change material 32 may be deposited over the lower electrode 22 and the insulator 30. A suitable conductive region may be deposited over the deposited lower electrode 22 to form the upper electrode 31 by patterning and etching the phase-change material 32/lower electrode 22 stack.

The memory cell 10 shown in Figure 1 may be replicated to form a memory array containing many cells. Such memory arrays can be used as the memory of a wide variety of processor-based systems, such as system 40 in Figure 9, or in processor-based appliances.

Figure 9 depicts one possible embodiment of a computer system 40 that might use a plurality of such memory cells, or memory array, in different configurations. The phase change memory 48 formed according to the principles described herein, may act as a system memory. The memory 48 may be coupled to an interface 44, for instance, which

in turn is coupled between a processor 42, a display 46 and a bus 50. The bus 50 in such an embodiment is coupled to an interface 52 that in turn is coupled to another bus 54.

5 The bus 54 may be coupled to a basic input/output system (BIOS) memory 62 and to a serial input/output (SIO) device 56. The device 56 may be coupled to a mouse 58 and a keyboard 60, for example. Of course, the architecture shown in Figure 9 is only an example of a potential architecture that may include the memory 48 using the
10 phase-change material.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended
15 claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: